25Gb/s 1V-driving CMOS ring modulator with integrated thermal tuning

Guoliang Li, Xuezhe Zheng, Jin Yao, Hiren Thacker, Ivan Shubin, Ying Luo, Kannan Raj, John E. Cunningham, and Ashok V. Krishnamoorthy

Oracle Labs, Oracle, San Diego, CA 92121, USA
glenn.li@oracle.com

Abstract: We report a high-speed ring modulator that fits many of the ideal qualities for optical interconnect in future exascale supercomputers. The device was fabricated in a 130nm SOI CMOS process, with 7.5µm ring radius. Its high-speed section, employing PN junction that works at carrier-depletion mode, enables 25Gb/s modulation and an extinction ratio >5dB with only 1V peak-to-peak driving. Its thermal tuning section allows the device to work in broad wavelength range, with a tuning efficiency of 0.19nm/mW. Based on microwave characterization and circuit modeling, the modulation energy is estimated ~7fJ/bit. The whole device fits in a compact 400µm^2 footprint.

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OCIS codes: (200.4650) Optical interconnects; (230.2090) Electro-optical devices; (250.7360) Modulators; (230.3120) Integrated optics devices; (250.5300) Photonic integrated circuits

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1. Introduction

It has now been widely recognized that interconnect power and density issues are among the biggest obstacles towards making exascale supercomputers [1-2]. Silicon photonics is expected to be an enabling technology for future exascale supercomputers by providing ultralow-power and ultrahigh-bandwidth-density inter-chip and intra-chip communications [3-4]. High-speed and efficient Si modulators are key components in the Si photonic links. To minimize the power consumption and footprint, the Si modulator has to be compact with very low capacitance and low voltage modulation. Many modulator candidates have been developed in the past few years, including carrier-injection Si ring modulators [5], Si microdisk modulators [6], Franz-Keldysh effect GeSi modulators [7], GeSi quantum well modulators [8], hybrid III-V modulators [9], and carrier-depletion Si ring modulators [10-12]. Among the various candidates, the carrier-depletion Si ring modulators employing reverse-biased PN diode have demonstrated all the desirable merits, including CMOS manufacturing compatibility, compact size (5μm radius), low driving voltage (1Vpp), low capacitance (<40fF), high speed (12.5Gb/s), low optical loss (~3dB ON-state loss), high extinction ratio (>7dB), and integrated thermal tuning. Most significantly, a 1x8 array of carrier-depletion CMOS Si ring modulators bonded to a 40nm CMOS driver chip has recently demonstrated 80Gb/s operation with ultralow power consumption averaged at <80fJ/bit including all the driver circuit power [13]. In addition, the ring resonator tuning power has also achieved remarkable 10-20 times reduction using Si substrate undercut and removal techniques, and demonstrated tuning efficiency of 2.4mW [14] and 3.9mW [15] per free spectral range (FSR). A statistical study on the CMOS foundry manufacturing data has indicated that ring resonators only needs to tune a small fraction of its FSR in a wavelength-multiplexed link (e.g., <1/8 of FSR for 8-wavelength link) [16]. All these exciting progress make the carrier-depletion Si ring modulator a very promising candidate for inter-chip communications. In this paper, we further report a 25Gb/s carrier-depletion CMOS ring modulator combined with integrated thermal tuning. Under a 1Vpp modulation without pre-emphasis, the output optical eye shows >5dB extinction ratio. Modulation energy is ~7fJ/bit when estimated using an extracted circuit model.

2. Device design and fabrication

In contrast to many ring mux/demux devices employing Si wire waveguides, our ring modulator uses a rib waveguide structure since a Si slab is needed to connect the optical waveguide to the electrodes for applying electrical modulation. Fig.1 shows a cross-section diagram of the ring waveguide in the high-speed modulation section. Several tradeoffs have to be considered in determining the waveguide dimensions. For example, we have to tradeoff the electrical properties with the optical properties. To minimize resistance and capacitance, we would choose thicker Si slab and smaller waveguide height, which leads to a shallow-etched rib waveguide and expanded optical mode in the lateral direction; however, this would increase optical loss in the tight-bent ring and reduce optical confinement at the center of the waveguide. Another tradeoff example is between different optical properties: with fixed waveguide height and etch depth, minimizing optical bending loss would require a wider waveguide width; while maintaining single-mode operation would prefer a narrower

waveguide width. The ring radius plays a critical role in these tradeoffs, since it has strong impact to optical mode, as well as to device capacitance and resistance.

Our ring modulator chooses a 7.5μm waveguide radius in order to achieve a free spectral range (FSR) of ~12.8nm. This is designed for an 8-wavelength-channel WDM link with channel spacing of 1.6nm, so that eight ring modulators with incremental size difference would form a synthetic comb resonance uniformly covering the entire C-band [13]. This design can reduce tuning requirement for each ring to within 1/8 of FSR [16]. The choice of 7.5μm radius is also appropriate for achieving small capacitance while providing enough space for integrating thermal resistor tuning section. The ring waveguide is designed as 380nm wide, with 220nm etch depth and 80nm thick Si slab, as shown in Fig.1. The bus waveguide is made narrower (300nm) for safe single-mode operation as well as better bus-ring coupling control [17].

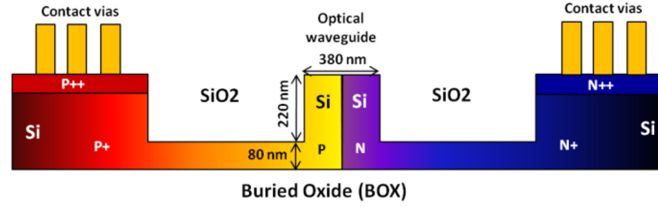

Fig.1. Cross-section diagram of the ring waveguide high-speed section. The color shading represents doping density variations from low (light colors) to high (dark colors).

In addition to the ring waveguide dimensions, another important design space is the PN junction doping. A symmetric lateral PN junction is employed in the high-speed modulation waveguide. An ideal doping profile in the optical waveguide would be vertically uniform while laterally increasing density at locations farther away from the PN junction. The goal is to achieve small capacitance, small resistance, small optical loss, but good phase modulation simultaneously. An important factor that must be considered in the design is impurities diffusion occurred during implantations and multiple CMOS thermal cycles. Process and implant simulations have been carried out to determine implant recipes for different regions in order to achieve the desired doping profile after impurities diffusion.

In the design of doping profile, the most important parameter is the target doping density at the diode junction located at the center of the waveguide. Note that the junction doping profile is linear-graded instead of abrupt due to the implant diffusion. The actual impurity densities at both P and N sides decrease linearly from the target N_d to zero at the center of the junction [18]. The PN junction doping determines the depletion width, and it overlaps with the center of the optical mode, therefore it has significant impact to the modulation depth and optical loss. The optical loss, in turn, determines the quality factor of the ring and the photon-lifetime-limited modulation bandwidth. A simple mathematic formula can help to better understand the impact of the junction doping to the modulation depth:

$$\frac{\Delta\lambda_{shift}}{\Delta\lambda_{FWHM}} \propto \frac{N_d^{1/3}}{\alpha_{dop}+\alpha_{other}}, \quad \text{where } \alpha_{dop} \propto N_d \tag{1}$$

In the above formula, $\Delta\lambda_{shift}$ is the resonance wavelength shift under voltage swing, which is proportional to $(N_d)^{1/3}$ in a linear-graded PN junction; $\Delta\lambda_{FWHM}$ is full width at half maximum (FWHM) of the resonance width, which is proportional to the waveguide loss coefficient $\alpha=\alpha_{dop}+\alpha_{other}$, where α_{dop} is due to junction doping and is roughly proportional to N_d, and α_{other} is due to other mechanisms such as waveguide scattering loss, bending loss and free-carrier absorption loss outside of the junction area (with higher doping densities). According to the above formula, if we choose N_d to make $\alpha_{dop} = 0.5\alpha_{other}$, we can maximize $\Delta\lambda_{shift}/\Delta\lambda_{FWHM}$, thus maximize modulation depth. Typical α_{other} is ~6dB/cm, thus optimized α_{dop} should be 3dB/cm, which requires a relatively low junction doping of ~$3\text{x}10^{17}$ cm^{-3}.

On the other hand, under critical coupling condition, the photon-lifetime-limited modulator bandwidth is proportional to the waveguide loss, $f_O=c\alpha/(\pi n_g)$, where c is the light speed in vacuum, $\alpha=\alpha_{dop}+\alpha_{other}$, and n_g~4.0 is the optical group velocity. The above optimized junction doping for maximized modulation depth results in a small α of 9dB/cm, which limits the bandwidth to 5GHz due to photon lifetime. Therefore, for higher bandwidth above 10GHz, we need to increase the junction doping density and sacrifice the modulation depth. To get quantitative relationships, we simulated the resonance wavelength shift ($\Delta\lambda_{shift}$), photon-lifetime-limited bandwidth (f_O), quality factor $Q=c/(\lambda f_O)$, and modulator penalty, at different junction doping densities, and plot the results in Fig.2. Here the modulator penalty (for voltage swing from -0.5V to 0.5V) includes the loss of averaged optical power between modulator input and output, which would be 3dB for an ideal modulator, and power penalty due to limited extinction ratio. Fig.2 indicates that to have f_O>25GHz, Q has to be <8000, $\Delta\lambda_{shift}$ would be >40pm, but modulator penalty would be >9dB.

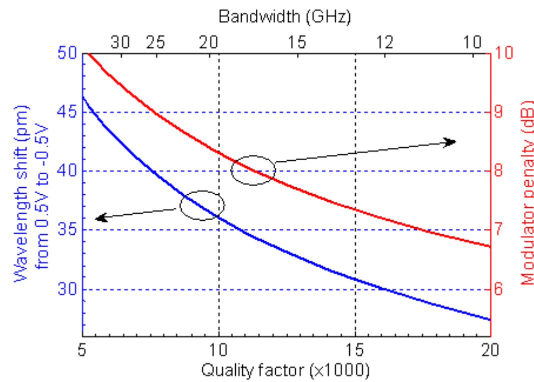

Fig 2: Relationships between ring resonator Q, photon-lifetime-limited bandwidth, resonance wavelength shift, and modulator penalty. The hidden variable is the PN junction doping density. Critical coupling condition and 100% diode coverage of the ring are assumed.

Our ring modulator was fabricated with Luxtera/Freescale's 130nm CMOS Photonics technology. Fig.3 shows a photograph of the fabricated device. The device layout has been optimized for high-speed modulation using Luxtera's PDK tools. 67% of the ring is made as PN diode for high-speed modulation, with a target junction doping density of $3\text{x}10^{18}$ cm^{-3}; while the upper-right 25% is N-type doped as a Si resistor for thermal tuning. There are 2µm-wide isolation gaps, where the ring waveguide is undoped, between the PN diode and the thermal resistor sections. Multiple metal layers are used for the layout of electrodes. The whole device, excluding probing-pads-associated metals, fits in a compact $400\mu m^2$ footprint.

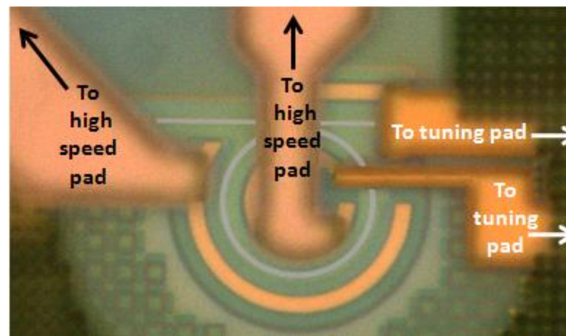

Fig 3: Photograph of the ring modulator. The upper-right 25% of the ring is made as a Si resistor heater providing wavelength tuning.

3. Device DC performance

Fig. 4(a) shows the measured resonant spectrum with different DC voltages applied across the high-speed pads, which results in reverse bias to the PN diode. The measured quality factor Q is ~8,000 at 0V. The resulted resonant wavelength shift at different bias voltages is plotted in Fig. 4(b). In a linear-graded PN junction, assuming the optical mode is laterally uniform in the depletion region, it can be derived that the resonant wavelength shift is proportional to $(V_b-V)^{2/3}$, where V is the applied voltage (negative for reverse bias), and V_b is the junction built-in voltage [18]. In our device V_b is estimated to be ~0.95V and slightly changes with the applied voltage. Both the theoretical dependence and the measured results in Fig. 4(b) indicate that the resonance shift efficiency is better at slightly positive bias. However, a positive bias beyond 0.5V will make the diode close to turn-on condition, which will significantly increase the diode capacitance and lower the modulation speed. With voltage changes from 0.5V to -0.5V, we achieved a 26pm resonance shift, which is less that the 40pm shift shown in Fig. 2 (with a Q of 8,000) due to only 67% diode coverage in the actual device.

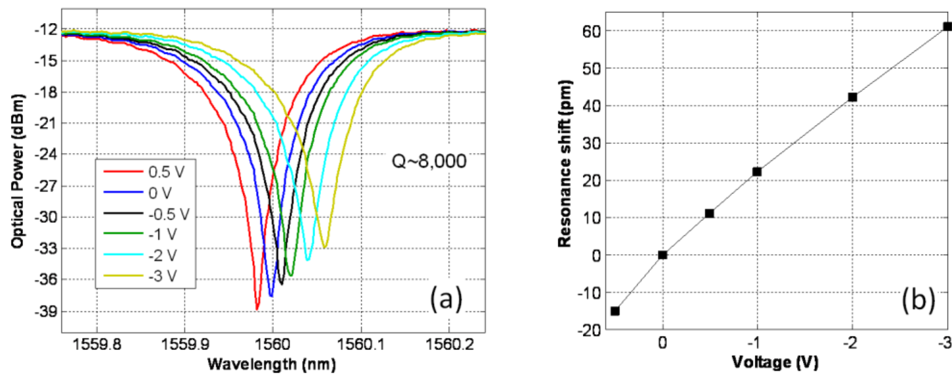

Fig 4: (a) Resonant spectrum with different voltages applied to the PN diode. (b) Resonance wavelength shift (relative to 0V) at different bias voltages.

Thermal tuning efficiency has been tested by applying different tuning power to the integrated Si resistor. Fig. 5(a) shows the resonant spectrum with different tuning power. The Si resistor has a resistance of 750Ω. The resonant wavelength versus tuning power is plotted in Fig. 5(b), showing a tuning efficiency of 0.19nm/mW, thus 66mW tuning power is needed to tune the whole 12.6nm FSR. With backside local substrate removal technique, up to 20 times enhancement of tuning efficiency is possible [15].

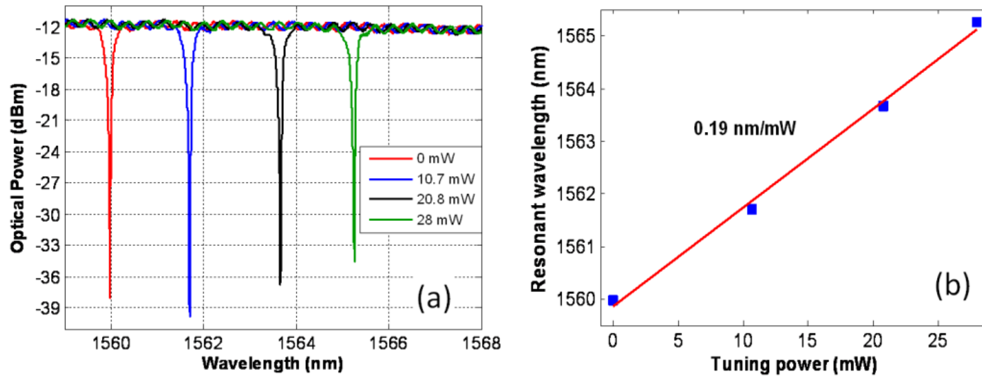

Fig.5. (a) Resonant spectrum with different tuning power applied to the Si resistor on the ring. (b) Resonant wavelength versus tuning power showing a 0.19nm/mW tuning efficiency.

4. Small-signal RF tests

The high-speed behavior of the ring modulator can be studied using a circuit model extracted by curve-fitting the measured S11 data [10]. The circuit model and the extracted circuit values at 0V are shown in Fig. 6(a). C_P denotes the capacitance between the electrodes through the top dielectrics, Rs and C_J model the current path through the reverse-biased PN junction, R_{Si} and C_{OX} model the current path through the BOX and the Si handle. Fig. 6(b) shows that excellent curve fitting is achieved. Based on this extracted circuit model, modulation energy is ~7fJ/bit when modulated by a 25Gb/s pseudo-random data with a 1V swing.

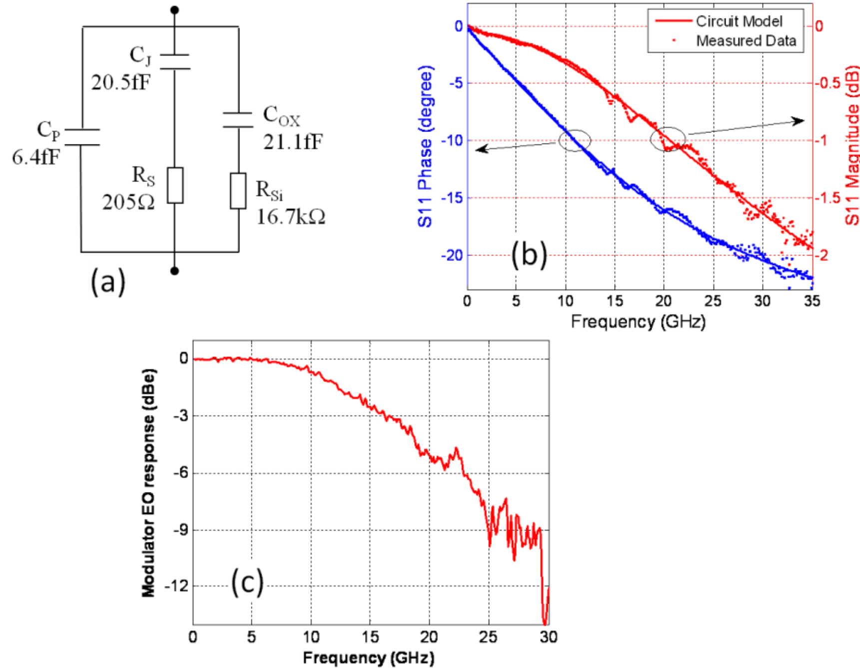

Fig.6. (a) Small-signal circuit model for the ring modulator with circuit values at 0V bias. (b) Curve-fitting of the measured S11 at 0V using the circuit model in (a). (c) Measured modulator EO (electrical-to-optical) frequency response at 0V.

The modulator frequency response was tested using a microwave network analyzer. The measured result in Fig. 6(c) indicates a 3dB bandwidth of 16.3 GHz at 0V and ~1560.03nm wavelength. The modulation bandwidth of the device is subject to both the RC limit, which is ~28GHz estimated from the circuit model (with a 50Ω source), and the photon lifetime limit, which is 24GHz based on the measured quality factor.

5. High-speed data modulation

To demonstrate high-speed modulation, we connect the high-speed pads of the ring modulator to a signal generator using a 40GHz electrical probe and a coax cable. To obtain 1Vpp driving voltage, the signal generator is set to swing from -0.25V to 0.25V. Due to the microwave reflection from the capacitive ring diode (see S11 in Fig. 6(b)), a reflected signal swing of approximately -0.25V to 0.25V is expected. The source signal and the reflected signal together construct a voltage modulation from -0.5V to 0.5V on the modulator diode. The optical bus waveguide of the ring modulator is terminated with two grating couplers, which are vertically coupled to an array of polarization maintaining (PM) fibers with cleaved end facets. The PM fiber at the input side is connected to a tunable laser, and the fiber at the output side goes to an EDFA and an optical filter to boost up the signal for eye-diagram

display. The amplified optical signal is fiber-connected to a 30GHz optical head on an Agilent digital scope. We first operate the ring modulator at 20Gb/s with 1Vpp driving in a PRBS31 data stream. The resulted optical eye is wide open with 7.6dB extinctin ratio, as shown in Fig. 7(a). The modulator is also capable of 25Gb/s modulation with 2Vpp driving, with signal generator set to swing from 0.5V to 1.5V (reverse bias). The resulted optical eye is shown in Fig. 7(b).

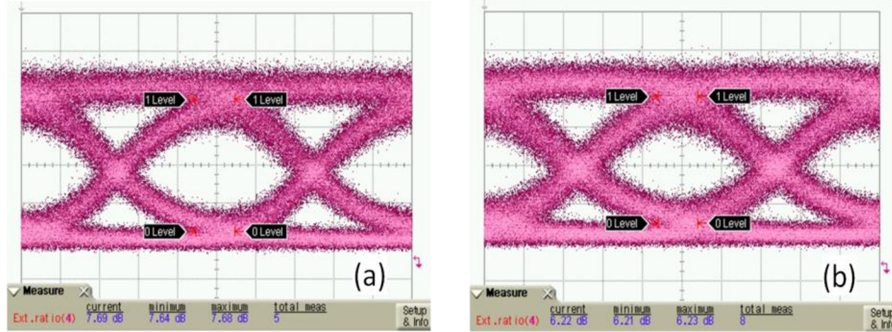

Fig.7. (a) 20Gb/s optical eye from the ring modulator with 1Vpp driving (time scale 10ps/div).
(b) 25Gb/s optical eye from the ring modulator with 2Vpp driving (time scale 8ps/div).

Next we try to demonstrate 25Gb/s modulation with 1Vpp driving. To also demonstrate modulation at different wavelengths, we use DC probes to contact the tuning pads of the device, and connect the probe to a DC power supply with monitored voltage and current. The measured eye-diagrams with 25Gb/s PRBS31 data modulation are shown in Fig. 8. Different tuning powers are applied to the integrated Si thermal resistor in order to tune the ring to modulate at different laser wavelengths. Although suffered some more eye-closure penalty compared with the eyes in Fig. 7, all the eyes in Fig. 8 are open with >5dB extinction ratio when the laser wavelength is tuned over the 5.3nm range, which proves that the device is capable of enabling error-free 25Gb/s communication with only 1V driving in a WDM link.

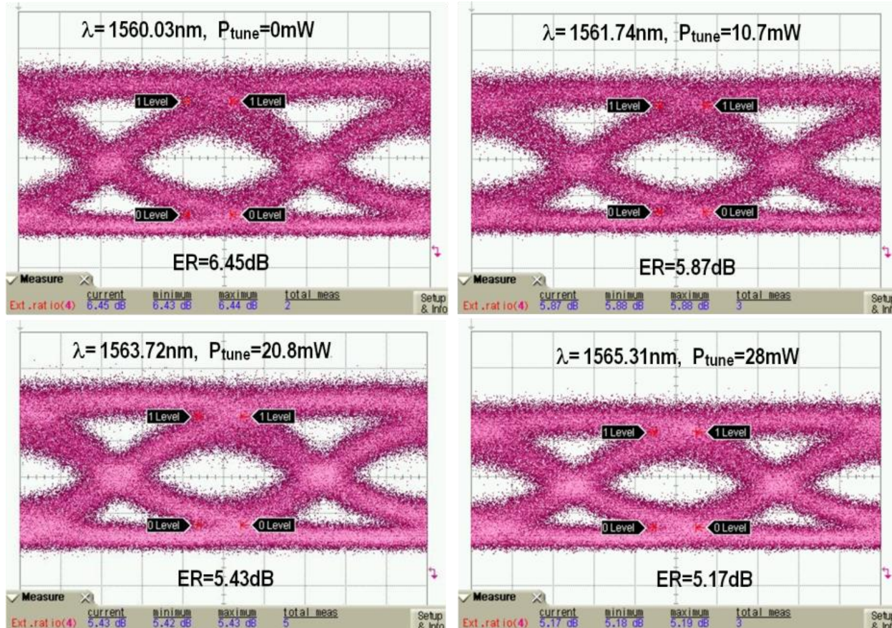

Fig.8. 25Gb/s optical eye from the ring modulator with 1V driving at different laser wavelengths with different tuning powers. The displayed time scale is 8ps/div.

6. Conclusions and acknowledgements

We have demonstrated an error-free 25Gb/s tunable carrier-depletion ring modulator with 7.5μm radius. The device was fabricated in a mainstream CMOS foundry. Its small junction capacitance leads to ultralow 7fJ/bit modulation energy with 1V driving at 25Gb/s. In a wide wavelength range, with tuning from the integrated thermal resistor, the modulator optical eye maintains open with >5dB extinction ratio when modulated by a 25Gb/s 1Vpp PRBS31 data stream. These results prove that carrier-depletion Si ring modulators can enable ultrahigh-speed and ultralow-power WDM photonic links with compact footprint, which is critical for future exascale computing systems. The authors thank Dr. Thierry Pinguet at Luxtera for his valuable support to our Si photonics tapeout. This work is supported, in part, by DARPA under Agreements HR0011-08-09-0001 and W911NF-07-1-0529. The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government. Approved for public release, distribution unlimited.